

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listings of Claims:

- 1 1. (original) A semiconductor data processing device
2 for connecting a non-volatile storage device to a general-
3 purpose bus of a host system, in which said data processing
4 device enters an active state or standby state in response
5 to a state of said general-purpose bus,
6 said data processing device comprising:
7 a clock circuit for stopping an internal clock signal
8 in said standby state; and
9 a voltage generation circuit for applying a substrate
10 bias voltage in a direction for reducing a threshold leak
11 current in said standby state.

- 1 2. (currently amended) The semiconductor data
2 processing device according to claim 1, further comprising:
3 a rewritable non-volatile memory for storing a control
4 program that connecting said non-volatile storage device to
5 said general-purpose bus; and

6 a central processing unit for executing said control
7 program,

8 wherein said central processing unit and said non-
9 volatile memory receive said substrate bias voltage.

1 3. (original) The semiconductor data processing
2 device according to claim 2, further comprising a circuit
3 for detecting the state of said general-purpose bus to
4 control state changes from said standby state to said
5 active state,

6 wherein said substrate bias voltage is not applied to
7 any of this circuit and said voltage generation circuit.

1 4. (original) The semiconductor data processing
2 device according to claim 3, further comprising a first
3 interface controller that interfaces with said non-volatile
4 storage device.

1 5. (original) The semiconductor data processing
2 device according to claim 4, further comprising a second
3 interface controller that interfaces with said general-
4 purpose bus.

1 6. (original) The semiconductor data processing
2 device according to claim 5,
3 wherein said first interface controller is a memory
4 card interface controller and said second interface
5 controller is a USB interface controller.

1 7. (currently amended) The semiconductor data
2 processing device according to claim 5 ~~or~~ 6, further
3 including a data transfer controller for controlling data
4 transfer between said first interface controller and said
5 second interface controller.

1 8. (original) The semiconductor data processing
2 device according to claim 7,
3 wherein said first and second interface controllers,
4 as well as said data transfer controller input/output
5 parallel data in units of 2^n bits while said central
6 processing unit inputs/outputs parallel data in units of n
7 bits or below.

1 9. (original) The semiconductor data processing
2 device according to claim 8,

3 wherein said data transfer controller is connected to
4 a 2n-bit first data bus while said central processing unit
5 is connected to either the lower part or upper part of said
6 first data bus.

1 10. (original) The semiconductor data processing
2 device according to claim 9,

3 wherein said first and second interface controllers
4 are connected to a 2n-bit second data bus respectively,

5 wherein said processing device further includes a
6 first data bus for connecting said first data bus to said
7 second data bus, and

8 wherein said bus controller fixes the correspondence
9 between each signal line of said second bus and the bit
10 position of access data and varies the correspondence
11 between each signal line of said first data bus and the bit
12 position of access data according to each access data size.

1 11. (original) A semiconductor data processing
2 device, comprising:

3 a central processing unit; and

4 a rewritable non-volatile memory for storing a program
5 to be executed by said central processing unit,

6 wherein an internal clock signal is stopped and a
7 substrate bias voltage is applied in a direction for
8 increasing a threshold voltage in the standby state, and
9 said substrate bias voltage is also applied to said central
10 processing unit and said non-volatile memory.

1 12. (currently amended) The semiconductor data
2 processing device according to claim 11, further
3 comprising:
4 first and second interface controllers controlled by
5 said central processing unit; and
6 a data transfer ~~controllers~~ controller capable of
7 controlling data transfer between said first and second
8 interface controllers.

1 13. (original) The semiconductor data processing
2 device according to claim 12,
3 wherein said first interface controller is a memory
4 card interface controller.

1 14. (original) The semiconductor data processing
2 device according to claim 12,

3 wh rein said second interface controller is a USB
4 interface controller.

1 15. (original) The semiconductor data processing
2 device according to claim 12,
3 wherein said first and second interface controllers,
4 as well as said data transfer controller input/output
5 parallel data in units of $2n$ bits while said central
6 processing unit inputs/outputs parallel data in units of n
7 bits or below.

1 16. (original) The semiconductor data processing
2 device according to claim 15,
3 wherein said data transfer controller is connected to
4 a $2n$ -bit first data bus while the central processing unit
5 is connected to either the lower or upper part of said
6 first data bus.

1 17. (original) The semiconductor data processing
2 device according to claim 16,
3 wherein said first and second interface controllers
4 are connected to a $2n$ -bit second data bus respectively,

5 wherein said processing device includes a bus
6 controller for connecting said first data bus to said
7 second data bus, and
8 wherein said bus controller fixes the correspondence
9 between each signal line of said second bus and the bit
10 position of access data and varies the correspondence
11 between each signal line of said first data bus and the bit
12 position of access data according to the access data size.

1 18. (original) A semiconductor data processing
2 device, comprising:
3 a first peripheral circuit that inputs/outputs
4 parallel data in units of $2n$ bits;
5 a second peripheral circuit that inputs/outputs
6 parallel data in units of $2n$ bits;
7 a data transfer controller capable of controlling data
8 transfer between said first and second peripheral circuits
9 that input/output data in parallel in units of $2n$ bits;
10 a $2n$ -bit first data bus connected to said data
11 transfer controller; and
12 a central processing unit that processes parallel data
13 in units of n bits or below, connected to either the lower
14 or upper part of said first data bus.

1 19. (original) The semiconductor data processing
2 device according to claim 18,
3 wherein said first and second peripheral circuits are
4 connected to said 2n-bit second data bus respectively, and
5 wherein said processing device further includes a bus
6 controller for connecting said first data bus to said
7 second data bus.

1 20. (original) The semiconductor data processing
2 device according to claim 19,
3 wherein said bus controller fixes the correspondence
4 between each signal line of said second bus and the bit
5 position of access data and varies the correspondence
6 between each signal line of said first data bus and the bit
7 position of access data according to each access data size.

1 21. (original) A data processing system comprising a
2 bridge circuit for connecting a non-volatile storage device
3 to a general-purpose bus,
4 wherein said bridge circuit includes a semiconductor
5 data processing device for controlling data transfer

6 between said general-purpose bus and said non-volatile
7 storage device,
8 wherein said semiconductor data processing device
9 includes a data transfer controller, a central processing
10 unit, and a rewritable non-volatile memory for storing a
11 control program, changes its state from active to standby
12 in response to the state of said general-purpose bus, and
13 stops an internal clock signal and applies a substrate bias
14 voltage in a direction for reducing a sub-threshold leak in
15 said standby state to change the state from said standby to
16 said active in response to the second state that follows
17 said first state.

1 22. (original) The data processing system according
2 to claim 21,

3 wherein said substrate bias voltage is applied to said
4 central processing unit and said non-volatile memory in
5 said standby state.

1 23. (currently amended) The data processing system
2 according to claim 21 ~~or 22~~,

3 wherein said non-volatile storage device is a non-
4 volatile memory card, said general-purpose bus is a USB

5 bus, said first state is an idle state, and said second
6 state is a communication requesting state.

1 24. (original) A semiconductor data processing
2 device, comprising:
3 a central processing unit;
4 a non-volatile memory for storing a control program to
5 be executed in said central processing unit, said memory
6 capable of writing and erasing data therein/therefrom
7 electrically;
8 a clock generation circuit; and
9 a first control circuit,
10 wherein said clock generation circuit stops generation
11 of said clock when said data processing device enters said
12 standby state while said first control circuit controls
13 said central processing unit, said non-volatile memory, and
14 said clock generation circuit so as to reduce a sub-
15 threshold leak current in each MOS transistor constituting
16 said central processing unit, said non-volatile memory, and
17 said clock generation circuit.

1 25. (original) The semiconductor data processing
2 device according to claim 24,

3 wherein said first control circuit receives first and
4 second supply potentials to be driven to operate regardless
5 of whether said data processing device is in said standby
6 state or not.

1 26. (original) The semiconductor data processing
2 device according to claim 25, further including a
3 peripheral circuit,

4 wherein said peripheral circuit includes a first
5 detection circuit for detecting the state of a bus to which
6 it is be connected,

7 wherein said first control circuit controls the
8 elements of said peripheral circuit except for said first
9 detection circuit in response to said standby state, and

10 wherein said first detection circuit receives first
11 and second supply potentials to be driven to operate
12 regardless of whether or not said data processing device is
13 in said standby state.

1 27. (original) The semiconductor data processing
2 device according to claim 26,

3 wherein said processing device further includes a
4 second control circuit,

5 wherein said second control circuit includes a second
6 detection circuit for detecting the output of said first
7 detection circuit,

8 wherein said first control circuit controls circuit
9 elements of said second control circuit other than said
10 second detection circuit in response to said standby state,
11 and

12 wherein said second detection circuit receives said
13 first and second supply potentials to be driven to operate
14 regardless of whether or not said data processing device is
15 in said standby state.

1 28. (original) A data processing system comprising a
2 bridge circuit for connecting a non-volatile storage device
3 to a general-purpose bus,

4 wherein said bridge circuit includes a semiconductor
5 data processing device for controlling data transfer
6 between said general-purpose bus and said non-volatile
7 storage device,

8 wherein said semiconductor data processing device
9 includes a data transfer controller, a central processing
10 unit, a rewritable non-volatile memory for storing a
11 control program to be executed in said central processing

12 unit, a clock generation circuit, and a first control
13 circuit,
14 wherein said semiconductor data processing device
15 changes the state from said standby to said active in
16 response to the first state of said general-purpose bus,
17 wherein said clock generation circuit stops generation
18 of said clock signal in said standby state,
19 wherein said control circuit controls said central
20 processing unit, said non-volatile memory, and said clock
21 generation circuit so as to reduce the sub-threshold leak
22 current of each MOS transistor constituting said central
23 processing unit, said non-volatile memory, and said clock
24 generation circuit, and
25 wherein said semiconductor data processing device
26 changes the state from said standby to said active in
27 response to the second state of said general-purpose bus,
28 said second state following said first state.

1 29. (original) The data processing system according
2 to claim 28,

3 wherein said first control circuit of said
4 semiconductor data processing device receives said first
5 and second supply potentials and is driven to operate

6 regardless of whether or not said data processing device is
7 in said standby state.

1 30. (original) The data processing system according
2 to claim 29,
3 wherein said semiconductor data processing device
4 further includes a peripheral circuit,
5 wherein said peripheral circuit includes a first
6 detection circuit for detecting the state of said general-
7 purpose bus,
8 wherein said first control circuit controls elements
9 of said peripheral circuit except for said first detection
10 circuit in response to said standby state, and
11 wherein said first detection circuit receives said
12 first and second supply potentials and is driven to operate
13 regardless of said standby state.

1 31. (original) The data processing system according
2 to claim 26,
3 wherein said semiconductor data processing device
4 further includes a second control circuit,

5 wherein said second control circuit includes a second
6 detection circuit for detecting the state of said first
7 detection circuit,
8 wherein said first control circuit controls elements
9 of said second control circuit except for said second
10 detection circuit in response to said standby state, and
11 wherein said second detection circuit receives said
12 first and second supply potentials and is driven to operate
13 regardless of said standby state.

1 32. (new) The semiconductor data processing device
2 according to claim 6, further including a data transfer
3 controller for controlling data transfer between said first
4 interface controller and said second interface controller.

1 33. (new) The semiconductor data processing device
2 according to claim 32,
3 wherein said first and second interface controllers,
4 as well as said data transfer controller input/output
5 parallel data in units of 2^n bits while said central
6 processing unit inputs/outputs parallel data in units of n
7 bits or below.

1 34. (new) The semiconductor data processing device

2 according to claim 33,

3 wherein said data transfer controller is connected to

4 a 2n-bit first data bus while said central processing unit

5 is connected to either the lower part or upper part of said

6 first data bus.

1 35. (new) The semiconductor data processing device

2 according to claim 34,

3 wherein said first and second interface controllers

4 are connected to a 2n-bit second data bus respectively,

5 wherein said processing device further includes a

6 first data bus for connecting said first data bus to said

7 second data bus, and

8 wherein said bus controller fixes the correspondence

9 between each signal line of said second bus and the bit

10 position of access data and varies the correspondence

11 between each signal line of said first data bus and the bit

12 position of access data according to each access data size.

1 36. (new) The data processing system according to

2 claim 22,

3 wherein said non-volatile storage device is a non-
4 volatile memory card, said general-purpose bus is a USB
5 bus, said first state is an idle state, and said second
6 state is a communication requesting state.